UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,181	04/20/2001	Hirotaka Ito	60188-065	1572

20277	7590	12/07/2004

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EXAMINER
PHAN, MAN U

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _20 April 2001_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-10_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-4,6 and 8-10_ is/are rejected.

7)☒ Claim(s) _5 and 7_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _20 April 2001_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All   b)☐ Some *   c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _04/20/01_.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

1.   The application of Ito et al. for a "Packet transmission/reception" filed 04/20/2001 has

been examined. This application claims foreign priority based on the application 2000-124867

filed April 25, 2000 in Japan. Receipt is acknowledged of papers submitted under 35 U.S.C

119(a) – (d), which papers have been placed of record in the file. Claims 1-10 are pending in the

application.

Drawings

2.   Figures 14-18 should be designated by a legend such as --Prior Art-- because only that

which is old is illustrated. See MPEP § 608.02(g).

A proposed drawing correction or corrected drawings are required in reply to the Office

action to avoid abandonment of the application. The objection to the drawings will not be held

in abeyance.

Claim Rejections - 35 USC ' 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth
>
> in section 102 of this title, if the differences between the subject matter sought to be patented and the
>
> prior art are such that the subject matter as a whole would have been obvious at the time the invention

was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability

shall not be negatived by the manner in which the invention was made.

4.   This application currently names joint inventors. In considering patentability of the claims

under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims

was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 1038

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5.   Claims 1-4, 6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Kobayashi et al. (US2003/0179719) in view of Sato (US#6,408,012).

With respect to claims 1, 8, 10, Kobayashi et al. (US2003/0179719) and Sato

(US#6,408,012) disclose a novel system and method for exchanging packetized data using

IEEE 1394 interface, according to the essential features of the claims. Kobayashi et al.

(US2003/0179719) discloses in Fig. 1 a block diagrams illustrated a part of the configuration of

a digital interface, in which a transmission/reception circuit 301 packetizes the information

data, supplied from a signal processing unit 106 provided in each device, into a communication

packet of a predetermined format. A transmission buffer 302 temporarily stores at least one

transmission packet supplied from the transmission/reception circuit 301. A reception buffer

303 temporarily stores at least a communication packet received through the port 1 or 2. A bus

resetting detection circuit 304 detects generation of a bus resetting, from a change in the bias

voltage applied to the port 1 or 2. A timer circuit 305 measures a time substantially coinciding

with that in other devices, in response to the cycle start packet 201 described in the foregoing.

A control circuit 306 controls the functions of various circuits constituting the digital interface

105 and those involved in the bus resetting (Page 4, para. [0094]).

Kobayashi et al. (US2003/0179719) differs from claims in that Kobayashi et al. does

not expressly disclose a link core circuit for receiving a packet externally delivered through a

bus, and sending out the packet to be transmitted, supplied from the packet processing

controller, by way of the bus. In the same field of endeavor, Sato (US#6,408,012) discloses in

Fig. 1 a block diagram illustrated the configuration of an MPEG use signal processing circuit

and IEEE 1394 serial interface, in which a link core circuit 101 is constituted by a transmission

circuit of an asynchronous communication use packet and an isochronous communication use

packet, a reception circuit, an interface circuit with the physical layer circuit 20 for directly

driving the IEEE 1394 serial bus BS of these packets, a cycle timer reset at every 125 .mu.s, a

cycle monitor, and a CRC circuit. The time data etc. of the cycle timer for example are supplied

to the isochronous communication system processing circuit through the CFR 111. The host

interface circuit 102 mainly performs interfacing of writing, reading, etc. of the asynchronous

communication use packet with the CPU 30 serving as the host computer and the transmission

use FIFO 104a and reception use FIFO 104b and interfacing of the transmission and reception

of various data with the CPU 30 and CFR 111 (Col. 4; lines 35 plus).

Regarding claims 2-4, 9, Kobayashi further teaches in Fig. 9 a block diagram illustrated an

example of the communication system which explained the procedure of identifying the

maximum transfer rates between a source and plural destinations and the procedure of

executing the data communication between a source and plural destinations by the

asynchronous transfer method of broadcast type (hereinafter called asynchronous broadcasting

transaction). As shown in Fig. 9, DVTR 103 functions as a source for transmitting information

data (including video data and audio data) to plural destinations, while the TV 101 functions as

a first destination for receiving and displaying such information data on the display unit 111,

the DVTR 102 functions as a second destination for receiving and recording such information

data on a recording medium such as a magnetic tape set in the deck unit 112, and the DVTR

103 functions as a controller for setting the logical connection relationship between the source

and the destinations. The signal processing unit 106 of the DVTR 103 divides the information

data, to be transmitted to plural destinations, into at least a data segment of a predetermined

data amount. Each segment data is packetized by the digital interface 105 of the DVTR 103

(more specifically the transmission/reception circuit 301 in the digital interface 105) into at

least a communication packet based on the asynchronous broadcast transaction method. In the

following description, the communication packet based on the asynchronous broadcast

transaction method is called an asynchronous broadcast packet. The data amount of each

segment data is variable, depending on the size of the reception buffer 303 secured at the

destination. Thus the DVTR 103 of the fourth embodiment determines the data amount of the

segment data, matching the smallest reception buffer size in the TV 101 and the DVTR 102.

Also the data amount transmittable in an asynchronous broadcast packet is variable, according

to the maximum transfer rate of the transmission path or the size of the transmission buffer 302

provided in the DVTR 103 (Page 9, para. [0209] –[0212]).

Regarding claim 6, Kobayashi further teaches in Fig. 14 the configuration of a packet

header 1419, in which a field 1401 (16 bits) indicates the destination ID which is the node ID

of the destination. In the communication protocol of the present embodiment, in order to realize

the asynchronous broadcast transaction, this field is set at a broadcasting ID (namely

"FFFF.sub.16"). The data block 1420 is composed of a header information (packet

information) 1421 and a data field 1422. A field 1411 (16 bits) indicates a connection ID,

storing for example a connection ID for identifying the logical connection relationship set

between the source and the destination. Each digital interface 105 identifies the necessary

packet based on the connection ID stored in this field (Page9; para. [0213] plus).

One skilled in the art would have recognized the need for effectively and efficiently

exchanging packetized data using IEEE 1394 interface, and would have applied Sato's novel

use of the signal processing circuit in a digital serial interface into Kobayashi's technique of

exchanging packetized data . Therefore, It would have been obvious to a person of ordinary

skill in the art at the time of the invention was made to apply Sato's signal processing circuit

into Kobayashi's method and apparatus for transmitting packets at a transfer rate that depends

on a response from a destination with the motivation being to provide a method and apparatus

for exchanging packetized data using an IEEE 1394 digital interface.

Allowable Subject Matter

6.   Claims 5 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

        The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest wherein the filter circuit predicts header information of a packet that the link core circuit should receive next time; compare the predicted header information to header information of a next packet that the link core circuit has actually received; determined, based on a result of the comparison, whether or not the next packet received by the link core circuit should be stored; and then supplies only the packets to be stored to the controller, as specifically recited in claim 5. Wherein the transaction control circuit manages a time it takes to transmit a packet after the controller started to make the packet or to finish processing a received packet after the controller received the packet, outputs a result of the time management to the CPU and also manages a time it takes for the CPU to transmit a packet after the CPU started to make the packet or to finish processing a received packet after the CPU received the packet, as specifically recited in claim 7.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Tanaka et al. (US#5,031,175) is cited to show the communication control method for releasing communication apparatus from occupied state.

The Tanaka et al. (US#6,023,475) is cited to show the data packet transmission method and apparatus for practicing the same.

The Joung et al. (US#6,754,222) is cited to show the packet switching apparatus and method in data network.

The Regev et al. (US#6,763,030) is cited to show the simplified switching hub for data communication networks.

The Hatae et al. (US#6,804,250) is cited to show the data communication system and node, and method of using the system and the node.

The Niida et al. (US#6,690,648) is cited to show the data communication apparatus, method, and system utilizing reception capability information of a destination node.

The Hatae et al. (US2003/0172201) is cited to show the data communication system, data communication method, and data communication apparatus.

8.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149.

The examiner can normally be reached on Mon - Fri from 6:00 to 3:00 EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (571) 272-2600.

9.   **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

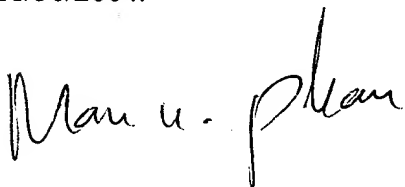**or faxed to:** (703) 305-9051, (for formal communications intended for entry)

Or: (703) 305-3988 (for informal or draft communications, please label

"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive,

Arlington. VA., Sixth Floor (Receptionist).

Mphan

11/30/2004.

MAN U. PHAN
PRIMARY EXAMINER